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14. ABSTRACT

A physics based model for GaN MESFETs is developed to determine the frequency dispersion of output resistance and transconductance due to traps. The equivalent circuit parameters are obtained by considering the physical mechanisms for current collapse and the associated trap dynamics. Detrapping time extracted from drain-lag measurements are 1.55 seconds and 58.42 seconds indicating trap levels at 0.69eV and 0.79eV, respectively. The dispersion frequency is in the range of MHz at elevated temperature, where a typical GaN power device may operate, although at room temperature it may be few Hz. For a 1.5 μm . 150 μm GaN MESFET with drain and gate biases of 10V and -1V respectively, 5% decrease in transconductance and 62% decrease in output resistance at RF frequencies from their DC values are observed. The dispersion characteristics are found to be bias dependent. A significant decrease in transconductance is observed when the device operates in the region where detrapping is significant. As gate bias approaches toward cutoff, the difference between output resistance at DC and that at RF increases. For drain and gate biases of 10V and -5V, output resistance decreases from 60.2 k. at DC to 7.5 k. at RF for a 1.5 μm . 150 μm GaN MESFET. This article was published in *IEEE Transactions on Electron Devices*, Vol. 51, No. 6, pp. 846-853, June 2004.

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A Physics-Based Frequency Dispersion Model of GaN MESFETs

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***Abstract*—A physics-based model for GaN MESFETs is developed to determine the frequency dispersion of output resistance and transconductance due to traps. The equivalent circuit parameters are obtained by considering the physical mechanisms for current collapse and the associated trap dynamics. Detrapping time extracted from drain-lag measurements are 1.55 and 58.42 s indicating trap levels at 0.69 and 0.79 eV, respectively. The dispersion frequency is in the range of megahertz at elevated temperature, where a typical GaN power device may operate, although at room temperature it may be few hertz. For a 1.5 × 150 μm GaN MESFET with drain and gate biases of 10 V and −1 V, respectively, 5% decrease in transconductance and 62% decrease in output resistance at radio frequencies (RFs) from their DC values are observed. The dispersion characteristics are found to be bias dependent. A significant decrease in transconductance is observed when the device operates in the region where detrapping is significant. As gate bias approaches toward cutoff, the difference between output resistance at dc and that at RF increases. For drain and gate biases of 10 and −5 V, output resistance decreases from 60.2 kΩ at dc to 7.5 kΩ at RF for a 1.5 μm × 150 GaN MESFET.**

***Index Terms*—Current collapse, detrapping time, frequency dispersion, GaN MESFET.**

I. Introduction

GaN-BASED heterojunction field effect transistors (FETs) that offer a high bandgap energy of 3.4 eV and a high breakdown electric field of 2.7×10^6 V/cm [1] are highly attractive for high-power and high-temperature applications at microwave frequencies. Recently, GaN HEMTs with a power output up to 9.8 W/mm at 8 GHz [2] have been demonstrated. With SiC as a substrate, GaN FETs have been operated up to 750 °C, as has been demonstrated by Daumiller *et al.* [3]. With a high electron saturation velocity of 2.7×10^7 cm/s [4] and low dielectric constant with a commensurate lower capacitance, GaN-based devices are potential choices for high-frequency operation. GaN HEMT with $f_T = 101$ GHz and $f_{max} = 155$ GHz has also been demonstrated [5].

GaN-based devices are plagued with traps that lead to current collapse in the cureent–voltage (*I–V*) characteristics [6]–[9], which results in severe performance degradation at high-power and high-frequency applications. Zhang *et al.* [6] reported current collapse in epitaxially grown GaN junction FETs at high drain bias and proposed an estimation of the length of the trapped charge region along the channel, at the channel–substrate interface. Klein *et al.* [7] have reported current collapse in GaN MESFETs in the absence of light. They also presented a theoretical model describing the optical restoration of the collapsed drain current at low drain bias. Binari *et al.* [8] have reported current collapse at moderately high drain bias in GaN HEMTs. Kunihiro *et al.* [9] have reported recovery of current collapse with measurements with 10 s hold time as the electrons get more time to be detrapped. At high frequencies, when the detrapping time is comparable to or greater than the signal period, traps cannot respond quickly enough to the applied voltage giving rise to frequency dispersion in device transconductance and output resistance [10], [11].

For microwave circuit design, the frequency dispersion of electrical characteristics is important, as trapping effects reduce the transconductance and output resistance significantly from their dc values. Moreover, the large-signal device models required to design analog and mixed-signal and high-power circuits must include dc to radio frequency (RF) dispersion of the device characteristics for accurate analysis [10], [12]–[14]. Golio *et al.* [12] used an additional voltage-dependent current source in an *RC* network to account for the frequency dispersion of transconductance and output resistance in GaAs MESFETs. Ytterdal *et al.* [13] reported an AlGaAs–GaAs heterostructure FET model suitable for mixed-mode circuit design incorporating frequency dispersion of transconductance and output resistance. In these works, the circuit parameters were extracted from experimental data. Lee *et al.* [10] reported a physics-based model to address frequency dispersion in GaAs MESFETs due to deep-level traps by obtaining the self-backgating parameters from experimental data. Larson [14] proposed an improved circuit model to incorporate the bias dependence of output resistance dispersion. As discussed, the determination of frequency dispersion of output resistance and transconductance has been based upon extracting circuit parameters from experimental data and not on physical principles describing trapping effects. In this paper, the applied bias, detrapping time, and temperature dependences of frequency dispersion of output resistance and transconductance are investigated by formulating the equivalent circuit parameters of the intrinsic GaN MESFET obtained mainly from the underlying physics of the device.

II. Theory

The effect of carrier trapping on frequency dispersion of output resistance and transconductance is incorporated in Fig. 1. Following the treatment reported by Golio *et al.* [12],

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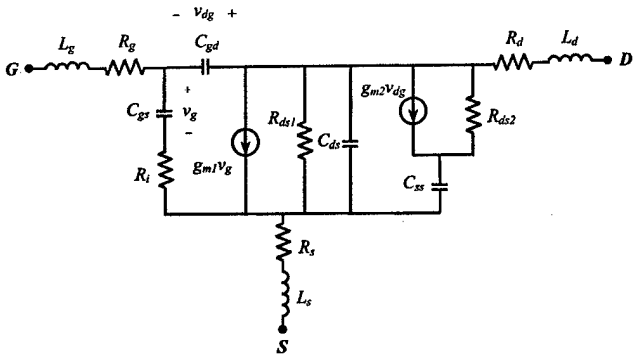

Circuit element	$V_{GS}=-1$V	$V_{GS}=-3$V
g_{m1} (mS)	6.91	4.89
g_{m2} (mS)	0.047	0.035
R_{ds1} (Ω)	7124	9768
R_{ds2} (Ω)	3.7×10^9	4.7×10^9
C_{gs} (fF)	100.8	80.7
C_{gd} (fF)	44.7	43.8
C_{ss} (fF)	100.8	80.7
C_{ds} (fF)	40.0	40.0
R_i (Ω)	24	20
R_g (Ω)	6.0	6.0
R_s (Ω)	90.0	90.0
R_d (Ω)	70.0	70.0
L_g (nH)	0.055	0.055
L_s (nH)	0.027	0.027
L_d (nH)	0.307	0.307

Fig. 1. GaN MESFET circuit model. Parameters for 1.5 × 150 μm GaN MESFET with V_{DS} = 25 V and V_{GS} = −1 and −3 V are shown in the table.

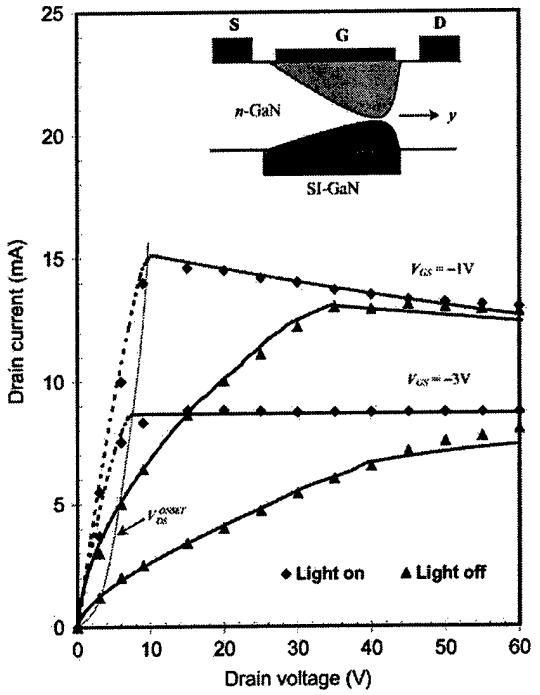

Fig. 2. *I–V* characteristics (V_{GS} = −1 and −3 V) considering trapping effects. Calculated and measured results are shown by solid lines and symbols, respectively [18]. The inset shows the depletion regions in the GaN MESFETs when carriers are captured by the substrate traps.

the effects of traps are incorporated through the parameters g_{m2}, R_{ds2}, and C_{ss}. These parameters are obtained once the underlying physical processes governing trap dynamics are formulated. Intrinsic circuit parameters $C_{gs}, C_{gd}, g_{m1}, R_i$, and R_{ds1} are obtained from conventional small-signal MESFET analysis in the absence of traps. Calculated *I–V* characteristics, as shown in Fig. 2, are based upon a physical mechanism for current collapse and restoration proposed by the present authors in [15]. At high drain bias, the electrons are captured by the traps located in the substrate, forming a second depletion layer in the channel at the channel–substrate interface as shown in the inset of Fig. 2. This depletion layer gradually disappears with increasing drain bias, as the detrapping process is initiated on the subsequent *I–V* trace. The thicknesses of the depletion layer in the channel under the gate due to an applied gate bias V_{GS} is $h(y) = \sqrt{(2\varepsilon/qn_c)[V_{bi} + V(y) + V_{GS}]}$ and that at the channel–substrate interface due to captured electrons is $x_n(y) = \sqrt{(2\varepsilon/qn_c)(1/(1+n_c/N_T))[U_{bi} + V(y)]}$, where $V_{bi} = (kT/q)\ln(n_c/n_i)$ is the built-in potential of the metal–semiconductor junction, $U_{bi} = (kT/q)\ln(n_c N_T/n_i^2)$ is the built-in potential of the channel–substrate junction, $V(y)$ is the potential along the channel at y ($y = 0$ at the source) due to V_{DS}, N_T is the occupied trap concentration at the channel–substrate interface, n_i is the intrinsic carrier concentration, ε is the GaN dielectric constant, q is the electronic charge, k is the Boltzmann constant, T is the temperature in Kelvin, and n_c is the channel electron concentration. n_c equals the summation of the doping concentration in the channel N_d and the carriers recovered due to detrapping for a given V_{DS}. Drain current can be expressed as $I_D = qWn_c\mu_n E(y)[d - h(y) - x_n(y)]$ where μ_n is the electron mobility, d is the thickness of the channel, W is the width of the device, and $E(y) = dV(y)/dy$ is the electric field along the channel. Integrating I_D over gate length L (between $y = 0$ and $y = L$), the drain current is expressed in the following form:

$$I_D = I_P\left\{3\left(u_d^2 - u_0^2\right) - 2\left(u_d^3 - u_0^3\right) - 2[1 + n_c \cdot (V_{DS})/N_T(V_{DS})]\left(x_d^3 - x_0^3\right)\right\}, \quad V_{DS} \le V_{DS,sat} \quad (1)$$

where

$$\begin{aligned} I_P &= q^2 n_c^2 \mu_n W d^3/6\varepsilon L \\ u_d &= \sqrt{(V_{bi} + V_{DS} - V_{GS})/V_{pi}} \\ u_0 &= \sqrt{(V_{bi} - V_{GS})/V_{pi}} \\ x_d &= \sqrt{(U_{bi} + V_{DS})/U_{pi}} \\ x_0 &= \sqrt{U_{bi}/U_{pi}} \\ V_{DS,sat} &= V_{pi}(u_s^2 - u_0^2) \\ V_{pi} &= qn_c d^2/2\varepsilon \\ U_{pi} &= qn_c d^2(1 + n_c/N_T)/2\varepsilon. \end{aligned}$$

To account for velocity saturation at the drain end of the channel at high drain bias, the saturation drain current is expressed in the following form:

$$I_D = qN_d v_{sat} W d\gamma(1 - u_s), \quad V_{DS} \ge V_{DS,sat} \quad (2)$$

where γ is the saturation factor, and $v_{\rm sat}$ is the electron saturation velocity. u_s is obtained by equating drain current expressions of (1) and (2) at $V_{\rm DS} = V_{\rm DS,sat}$.

A. Determination of Intrinsic Model Parameters

Intrinsic circuit parameters are obtained from (1) in the absence of trapping effects (putting $n_c = N_d$ and dropping the last term in the $V_{\rm DS} \le V_{\rm DS,sat}$ region). Dividing the channel into linear (length $= L_1$) and saturation (length $= L - L_1$) regions to incorporate channel length modulation, the intrinsic transconductance g_{m1} is given by (3), shown at the bottom of the page, where $C_{11} = (\mu_n(1-u_0))/(\gamma v_{\rm sat}(1-u_1))$ and $C_{12} = (L_1)/(1-u_1) + (qN_d d^2 \mu_n u_1)/(\varepsilon\gamma v_{\rm sat})$. For a given gate and drain bias, L_1 and u_1 are calculated by simultaneously solving $L_1 = (qN_d d^2\mu_n)/(6\varepsilon\gamma v_{\rm sat}(1-u_1))[3(u_1^2-u_0^2) - 2(u_1^3-u_0^3)]$ and $V_{\rm pi}(u_1^2-u_0^2) + (2E_{\rm cr}du_1)/(\pi)\sinh[(\pi(L-L_1))/(2du_1)] = V_{\rm DS}$, which are obtained by equating drain currents at L_1 and solving Poission's equation in the depletion region. Intrinsic drain resistance $R_{\rm ds1}$ is given by (4), shown at the bottom of the page. Capacitances $C_{\rm gs}$ and $C_{\rm gd}$ are given by

$$C_{\rm gs} = \frac{WL}{2}\left(\frac{\varepsilon q N_d}{2V_{\rm bi}}\right)^{\frac{1}{2}}\left(1-\frac{V_{\rm GS}}{V_{\rm bi}}\right)^{-\frac{1}{2}} + \frac{\pi}{2}\varepsilon W \quad (5)$$

$$C_{\rm gd} = \frac{WL}{2}\left(\frac{\varepsilon q N_d}{2V_{\rm bi}}\right)^{\frac{1}{2}}\left(1-\frac{V_{\rm DG}}{V_{\rm bi}}\right)^{-\frac{1}{2}} + \frac{\pi}{2}\varepsilon W \quad (6)$$

where $V_{\rm DG}$ is the drain-to-gate voltage. The second term in (5) and (6) represents the contributions from drain and source sidewalls [16].

Intrinsic resistance is given by $R_i \approx (1/\eta g_{m1})$ where $\eta \approx 2[1 + (2\beta L_1)/(3(1-\beta)(L+L_{\rm gd}))]^2, \beta \approx (1/(\sqrt{1+2(V_{\rm GS}-V_{\rm OFF})\mu_n/Lv_{\rm sat}})$ and $L_{\rm gd}$ is the gate–drain separation [17]. The turn-off voltage $V_{\rm OFF}$ is estimated to be -6 V.

B. Determination of Trap-Related Circuit Parameters

The calculation of transconductance in the presence of traps g_{m2} requires an understanding of the detrapping processes at the channel–substrate interface. As shown in Fig. 2, the experimental data in the absence of light show current collapse and is attributed to the presence of traps at the channel–substrate interface. While in the presence of light, the trapped carriers are detrapped quickly, and no current collapse was observed [18]. It should be mentioned that current collapse was not observed in the first measurement at $V_{\rm GS} = 0$ V. However, current collapse was observed in subsequent measurements if the drain bias was over 30 V in previous measurements. As explained by the present authors, the observed characteristics can be explained by identifying acceptor traps with dual-energy states [15]. In GaN, the impurity responsible for carrier trapping that leads to dc current collapse has not been identified; however, it is highly likely that it is due to C, which may introduce multiple states within the band gap, and we refer to the two states as X^{+++} and X^{++} in this analysis. An electron transition from the valence band to the X^{+++} neutral state leads to the charge state X^{++} (reminiscent of the Cr states in GaAs). This capture of electrons in the buffer results in the formation of a negatively charged region at the channel–buffer interface consequently forming an additional depletion region at the channel–buffer interface causing drain current to decrease. With increasing drain bias, the transition of electrons from X^{++} level to the conduction band is facilitated as the X^{++} level moves closer to the quasi-Fermi level. The emission of electrons from the traps results in a decrease in the width of the depletion region at the channel–buffer interface with a consequent increase in drain current. At high drain bias ($V_{\rm DS} \ge 30$ V), carriers generated due to impact ionization are trapped, and the trap states become negatively charged, requiring a positively charged depletion region in the channel at the channel–substrate interface, and the process continues. Using the PISCES-II Device Modeling Program (Version 9009-Win32 × 86), the simulated electric field exceeded 1.0×10^6 V/cm for the structure reported by Binari *et al.* [18] for an applied drain bias of 30 V. Kunihiro *et al.* [9] have recently reported that in GaN, impact ionization is initiated at channel electric field around 0.4×10^6 V/cm; therefore, impact ionization in the structures reported by Bianri *et al.* [18] can be expected. With increasing drain bias, beyond $V_{\rm DS} \approx 5$ V, the quasi-Fermi level at the drain end of the channel comes closer

$$g_{m1} = \left.\frac{\partial I_D}{\partial V_{\rm GS}}\right|_{V_{\rm DS}} = \begin{cases} -\dfrac{W}{L}qN_d\mu_n d(u_d-u_0), & V_{\rm DS} \le V_{\rm DS,sat} \\ qN_d v_{\rm sat}\gamma W d\left\{1 - C_{11}E_{\rm cr}\cosh\left[\frac{\pi(L-L_1)}{2du_1}\right]\right\} & \\ \hline 2u_1V_{\rm pi} + \frac{2E_{\rm cr}d}{\pi}\sinh\left[\frac{\pi(L-L_1)}{2du_1}\right] - E_{\rm cr}\left(C_{12} + \frac{L-L_1}{u_1}\right)\cosh\left[\frac{\pi(L-L_1)}{2du_1}\right], & V_{\rm DS} \ge V_{\rm DS,sat} \end{cases} \quad (3)$$

$$R_{\rm ds1} = \frac{1}{\left.\frac{\partial I_D}{\partial V_{\rm DS}}\right|_{V_{\rm GS}}} = \begin{cases} \dfrac{L}{qN_d W d\mu_n(1-u_d)}, & V_{\rm DS} \le V_{\rm DS,sat} \\ \dfrac{1}{qN_d v_{\rm sat}\gamma W d}\left\{2u_1V_{\rm pi} + \dfrac{2E_{\rm cr}d}{\pi}\sinh\left[\dfrac{\pi(L-L_1)}{2du_1}\right] - E_{\rm cr}\left(C_{12} + \dfrac{L-L_1}{u_1}\right)\cosh\left[\dfrac{\pi(L-L_1)}{2du_1}\right]\right\} & \\ V_{\rm DS} \ge V_{\rm DS,sat} \end{cases} \quad (4)$$

to the trap level, thereby increasing the cross section of electron transition from the trap level to the conduction band. The initiation of electron detrapping reduces the width of the depletion region that results in an increase in drain current. Beyond $V_{DS} \approx 30$ V, impact ionization is initiated; the electrons are captured by the acceptor traps, and the process continues. The drain voltage at the onset of detrapping process (~5 V at $V_{GS} = -1$ V, from Fig. 2) is denoted as V_{DS}^{ONSET}, which decreases with decreasing V_{GS} as evident from Fig. 2. V_{DS}^{ONSET} is obtained by solving $(V_{bi}+V_{DS}^{ONSET}-V_{GS})^{1/2}+(1/(\sqrt{1+N_d/N_{t0}})(U_{bi}+V_{DS}^{ONSET})^{1/2} = \sqrt{(qN_dd^2/2\varepsilon)}$, which is obtained by applying the pinch-off condition to $(\partial I_D)/(\partial V_{DS})|_{V_{GS}} = 0$. To facilitate calculation, the computed V_{GS} dependence of V_{DS}^{ONSET} is approximated by the quadratic form $V_{DS}^{ONSET} = a_0 + a_1V_{GS} + a_2V_{GS}^2$ where $a_0 = 6.24$ V and $a_1 = 1.29$ and $a_2 = 0.03$ V^{-1}.

Theoretical calculations based upon the discussed model are compared with experimental data, in Fig. 2, to show good agreement. Calculations are carried out for a 1.5 μm × 150 μm GaN MESFET with 2000-Å n-GaN channel grown over a 3 μm semi-insulating (SI) GaN substrate. The channel doping concentration N_d is 2×10^{17} cm^{-3}. The measured low-field mobility μ_n is 410 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1} [7], [18]. The calculation is based upon the assumption that the drain bias dependence of trapped carrier concentration, in the drain bias range between V_{DS}^{ONSET} and the drain bias at the onset of impact ionization (~30 V at $V_{GS} = -1$ V), is $N_t = N_{to}\exp[-\alpha(V_{DS} - V_{DS}^{ONSET})]$. At the gate end of the drain the current due to the detrapping of carriers is modeled as $I_{Detrap} = qv_{sat}N_{to}Wd[1-\exp\{-\alpha(V_{DS}-V_{DS}^{ONSET})\}]$ where v_{sat} is the carrier saturation velocity in the channel. The fit with the measured *I–V* characteristics as shown in Fig. 2, is obtained with $N_{to} = 1.5 \times 10^{16}$ cm^{-3} and $\alpha = 0.112$ V^{-1}. The transconductance representing the effect of detrapping is obtained by differentiating the detrapping current with respect to V_{DG} as shown below

$$g_{m2} = qv_{sat}WdN_{to}\alpha\left[\frac{a_1 + 2a_2V_{GS}}{1 + a_1 + 2a_2V_{GS}}\right] \times \exp\left[-\alpha\left(V_{DS} - V_{DS}^{ONSET}\right)\right]. \quad (7)$$

By defining $\omega_{o(rds)}$ as $\omega_{o(rds)} = 1/t_d$ where $\omega_{o(rds)}$ is the frequency at which overall output resistance has decreased to the average of its low-frequency and the high-frequency values R_{ds2} is given by,

$$R_{ds2} \approx \frac{t_d}{C_{ss}(1 + g_{m2}R_{ds1})} \quad (8)$$

where t_d is the detrapping time constant. C_{ss} is comparable to C_{gs} [12] and the other circuit parameters are obtained from reported experimental data and are as follows: $R_g = 6\,\Omega$, $R_d = 70\,\Omega$, $R_s = 90\,\Omega$, and $C_{ds} = 0.040$ pF [18]. However, due to the unavailability of data for GaN-based devices, the inductances associated with connecting pads are assumed to be the same as those of GaAs FETs and are as follows: $L_g = 0.055$ nH, $L_d = 0.307$ nH, and $L_s = 0.027$ nH [12].

The determination of the detrapping time depends upon the nature and location of the traps. An estimation of t_d based upon the drain lag measurement reported by Binari *et al.* [8], for AlGaN–GaN HEMTs, is shown in Fig. 3. Assuming exponential decay of the detrapping current the detrapping time constant is estimated to be 53.2 s and is in agreement with the value mentioned in [8]. The detrapping time is expressed as [11]: $t_d \approx 1/\{\sigma_n v_{th} N_c \exp[-(E_c - E_t)/kT]\}$, where σ_n is the electron capture cross section, $v_{th} = \sqrt{3kT/m_e^*}$ is the thermal velocity, m_e^* is the electron effective mass in GaN, E_c and E_t are the conduction and trap energy levels, respectively. With $m_e^* \cong 0.2m_o$, where m_o is free electron mass, $N_c = 1 \times 10^{19}$ cm^{-3}, and $\sigma_n \cong 10^{-13}$ cm^{-2}, E_t is found to be located at 0.78 eV below E_c at room temperature. A better fit to the detrapping current, at 300 K, is obtained by using multiple time constants as shown in Fig. 3. The time constants of 58.42 and 1.55 s correspond to trap states located at 0.79 and 0.69 eV below E_c, respectively. As observed, these trap levels at room temperature correspond to dispersion frequencies of less than 1 Hz. However, with increasing temperature the dispersion frequency, due to the traps located at 0.79 and 0.69 eV, increases as shown in the inset and can be of the order of MHz at 600 K. Moreover, a higher dispersion frequency is possible due to the presence of other shallow traps. Although the estimated trap levels are based upon data reported for an AlGaN–GaN HEMT the calculated trap levels are consistent with the reported experimental values for GaN. Reported trap levels measured from the conduction band minimum are 0.59 and 0.66 eV [19], 0.598 and 0.67 eV [20], 0.59 and 0.88 eV [21], and 0.41–0.50 and 0.62–0.67 eV [22].

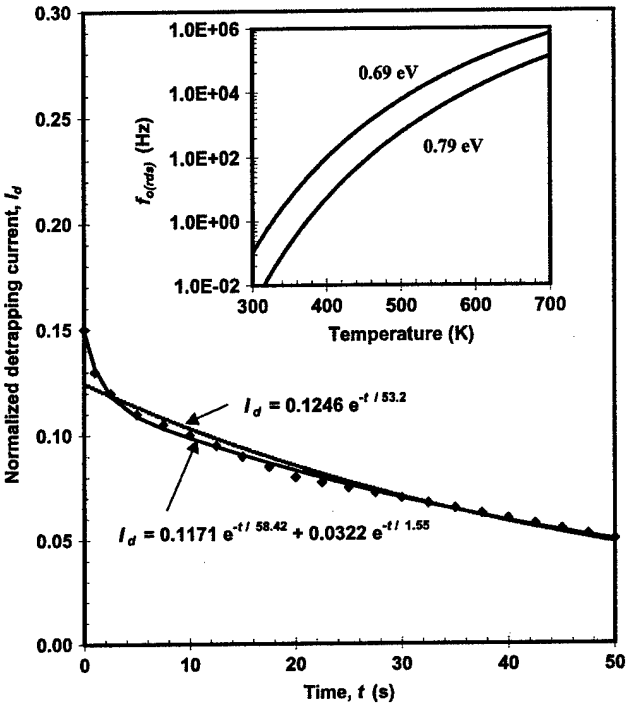

Fig. 3. Extracted detrapping current (symbols) from the drain lag measurement reported in [8]. Solid lines show the fits using single and multiple detrapping time constants [23]. Output resistance dispersion frequency ($f_{o(rds)}$) as a function of temperature is shown in the inset for different trap levels involved in the detrapping process.

Y-parameters, as listed in the Appendix, are calculated by placing short circuits at the output and input terminals of the

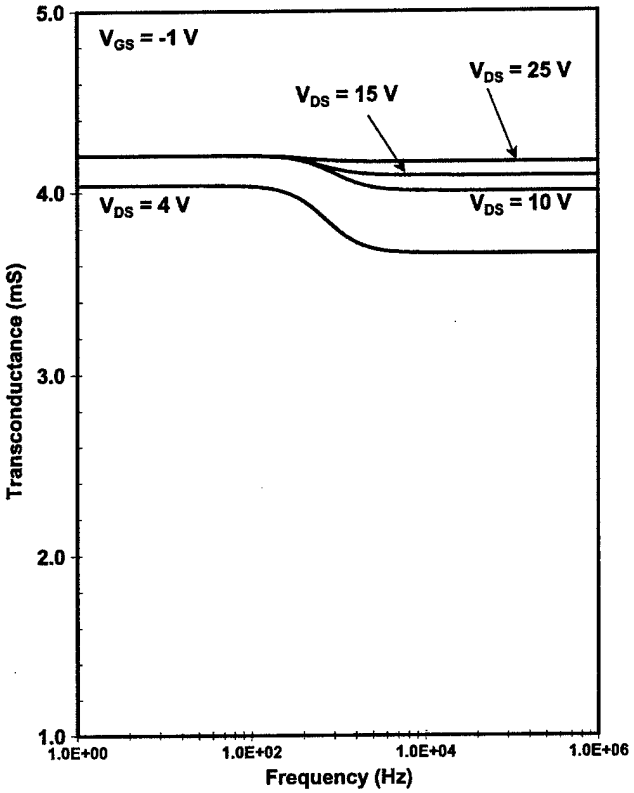

Fig. 4. Transconductance as function frequency with V_{DS} as parameter ($V_{GS} = -1$ V and detrapping time, $t_d = 0.5$ ms) [23].

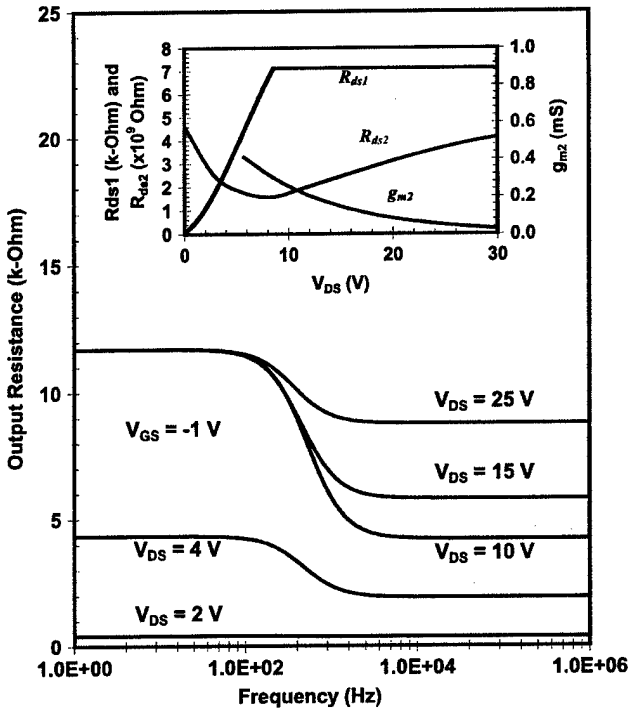

Fig. 5. Output resistance as function frequency with V_{DS} as parameter ($V_{GS} = -1$ V and detrapping time, $t_d = 0.5$ ms). Inset shows the variation of R_{ds1}, R_{ds2}, and g_{m2} as a function of V_{DS} for $V_{GS} = -1$ V [23].

circuit shown in Fig. 1. Y_{21} and Y_{22} are simplified at low and high frequencies to formulate the overall transconductance and output resistance.

III. Results and Discussion

Fig. 4 shows the variation of the overall device transconductance as a function frequency with drain voltage as parameter. The gate voltage is -1 V and the detrapping time is assumed to be 0.5 ms. For frequencies lower than $f_{o(gm)} \approx 1/2\pi R_{ds2} C_{ss}$, which is the dispersion frequency for transconductance [12], the overall transconductance equals $g_m^{LO} = (g_{m1}/1+g_{m1}R_s+(R_d+R_s/R_{ds1}))$ and for frequencies greater than $f_{o(gm)}$ the overall transconductance equals $g_m^{HI} \approx (g_{m1} - g_{m2}/1+g_{m1}R_s+g_{m2}R_d+(R_d+R_s)/(R_{ds1} \parallel R_{ds2}))$. The above expressions are obtained by simplifying Y_{21}. The overall transconductance increases with increasing V_{DS} until the saturation voltage is reached. The increase in the overall transconductance at low frequency is due to the increase in g_{m1} with increasing V_{DS} and the decrease at higher frequencies, for a given V_{DS}, is due to the contribution of g_{m2} as stated earlier. At elevated drain bias, most of the trapped electrons have already been released and the detrapping current is very small that results in a lower transconductance dispersion, which is also evident from (7).

Fig. 5 shows the frequency dispersion of output resistance with drain bias as parameter at $V_{GS} = -1$ V. For finite R_s and R_d the overall output resistance $R_{ds}^{LO} = R_s + R_d + R_{ds1}(1 + g_{m1}R_S)$ for frequencies less than the output resistance dispersion frequency $f_{o(rds)} \approx 1/2\pi t_d$. For frequencies greater than $f_{o(rds)}$, the overall output resistance $R_{ds}^{HI} \approx (R_{ds1} \| R_{ds2} \| 1/g_{m2})(1 + g_{m1}R_s + g_{m2}R_d + (R_d + R_s)/(R_{ds1} \parallel R_{ds2}))$. The above expressions are obtained by simplifying Y_{22}. At low V_{DS}, the output resistance does not show any dispersion and equals R_{ds}^{LO}. For frequencies lower than $f_{o(rds)} \approx 1/2\pi t_d$, only R_{ds1} contributes to the overall resistance as the branch containing C_{ss} behaves like an open circuit due to its high capacitive reactance. Moreover, with increasing V_{DS} the slope of the current-voltage characteristics decrease resulting in the observed increase in R_{ds}^{LO}. It is seen from (8) that R_{ds2} is always much larger than R_{ds1} and $1/g_{m2}$ (see inset of Fig. 5) and for frequencies greater than $f_{o(rds)}$ the overall output resistance is mainly determined by the parallel combination of R_{ds1} and $1/g_{m2}$. With increasing drain bias R_{ds1} increases and due to decreasing detrapping current g_{m2} decreases (see inset of Fig. 5). Therefore, dispersion of the output resistance is maximized at a certain drain bias beyond which dispersion decreases and the overall output resistance approaches R_{ds}^{LO} and is attributed to the diminishing values of g_{m2}. A similar behavior was observed in output resistance dispersion in GaAs FETs [13], [14].

Fig. 6 shows the dispersion in transconductance as a function of gate bias. The drain bias is 10 V and detrapping time is 0.5 ms. The overall low-frequency transconductance g_m^{LO} is governed by the behavior of g_{m1} which increases with increasing gate bias. The saturation of g_{m1} causes the observed rate of increase of g_m^{LO} with V_{GS} to decrease at higher gate bias. At higher frequencies, the overall transconductance dispersion $g_m^{LO} - g_m^{HI}$ is

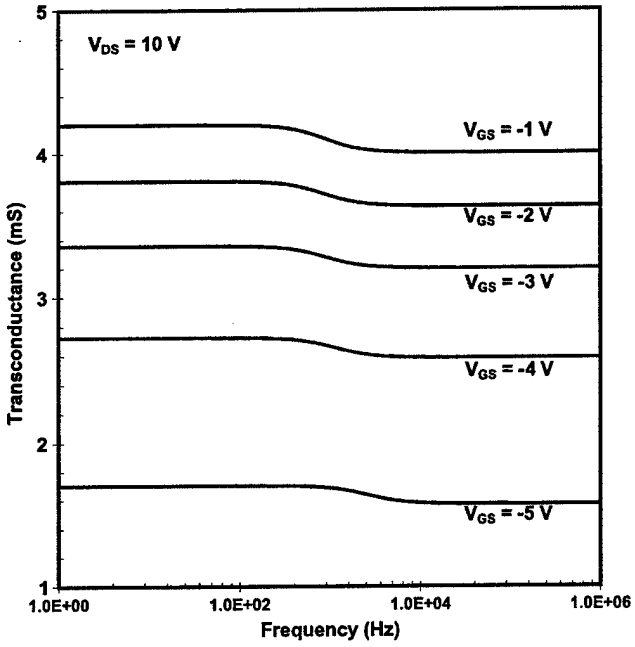

Fig. 6. Transconductance as function frequency with V_{GS} as parameter (V_{DS} = 10 V and detrapping time, t_d = 0.5 ms).

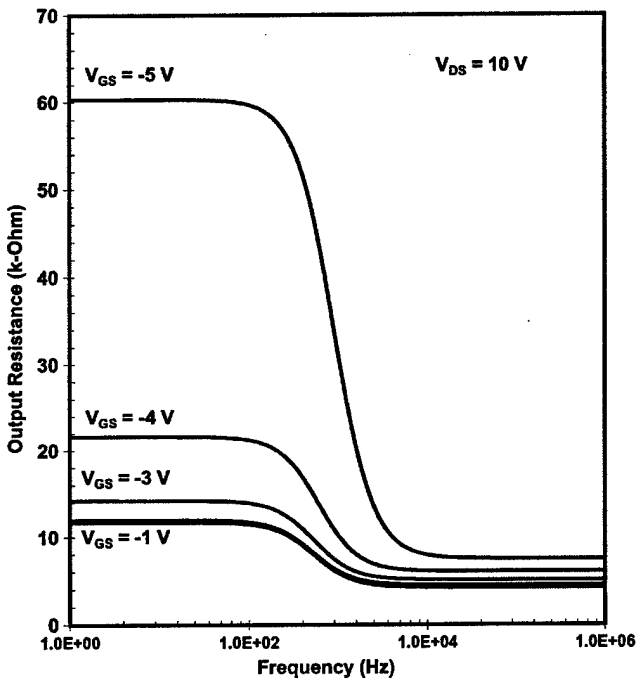

Fig. 7. Output resistance as function frequency with V_{GS} as parameter (V_{DS} = 10 V and detrapping time, t_d = 0.5 ms).

observed to decrease with increasing V_{GS}. This decrease is attributed to the effect of different resistive components in the circuit as evident from the expressions of g_m^{HI} and g_m^{LO}. It should be noted that with increasing V_{GS} although $g_m^{LO} - g_m^{HI}$ decreases, g_{m2} increases slightly due to an increase in V_{DS}^{ONSET}. Fig. 7 shows the dispersion of output resistance with varying gate bias. With decreasing gate bias, R_{ds1} increases and the parallel combination of R_{ds1}, $1/g_{m2}$ and R_{ds2} is dictated by $1/g_{m2}$ resulting in a higher dispersion.

IV. Conclusion

Frequency dispersion of transconductance and output resistance in GaN MESFETs is reported by considering the effect of traps. Detrapping time is estimated from drain-lag measurement data reported for AlGaN–GaN HEMT. The trap levels located at 0.69 and 0.79 eV are comparable to the experimental data reported for bulk GaN. The dispersion frequencies estimated from the trap levels are in the range of MHz at elevated temperatures, where a typical GaN power device may operate, although at room temperature it may be few Hz. In the linear region of operation, dispersion in transconductance is significant, whereas, dispersion in output resistance is crucial when the device operates near cutoff.

Appendix

Y-parameters of the circuit shown in Fig. 1, obtained by placing short circuits at the output and input terminals are as shown at the top of the next page, where

$$
\begin{aligned}
k_1 &= -Y_{gs} - Y_{m1} \\
k_2 &= -Y_{ds1} \\
k_3 &= Y_s + Y_{gs} + Y_{m1} + Y_{ds1} + Y_{ss} \\
k_4 &= -Y_{ss} \\
h_1 &= -Y_{gd} + Y_{m1} - Y_{m2} \\
h_2 &= Y_{gd} + Y_{ds1} + Y_{m2} + Y_{ds2} + Y_d \\
h_3 &= -Y_{m1} - Y_{ds1} \\
h_4 &= -Y_{ds2} \\
A_1 &= (Y_{gs} + Y_g + Y_{gd})/Y_{gs} \\
A_2 &= \frac{Y_{ss}(Y_{gs} + Y_g + Y_{gd}) - Y_{m2}Y_{gs}}{Y_{gs}(Y_{ss} + Y_{ds2})} \\
B_1 &= -Y_{gd}/Y_{gs} \\
B_2 &= \frac{Y_{gs}(Y_{ds2} + Y_{m2}) - Y_{gd}Y_{ss}}{Y_{gs}(Y_{ss} + Y_{ds2})} \\
C_1 &= -Y_g/Y_{gs} \\
C_2 &= -\frac{Y_g Y_{ss}}{Y_{gs}(Y_{ss} + Y_{ds2})} \\
Y_{m1} &= g_{m1}/(1 + j\omega C_{gs} R_i) \\
Y_{m2} &= g_{m2} \\
Y_g &= 1/(R_g + j\omega L_g) \\
Y_s &= 1/(R_s + j\omega L_s) \\
Y_d &= 1/(R_d + j\omega L_d) \\
Y_{gs} &= j\omega C_{gs}/(1 + j\omega C_{gs} R_i) \\
Y_{gd} &= j\omega C_{gd} \\
Y_{ss} &= j\omega C_{ss} \\
Y_{ds1} &= (1 + j\omega C_{ds} R_{ds1})/R_{ds1} \\
Y_{ds2} &= 1/R_{ds2}.
\end{aligned}
$$

$$Y_{11} = Y_g \left[1 + \frac{(k_3C_1 + k_4C_2)(h_2 + h_3B_1 + h_4B_2) - (h_3C_1 + h_4C_2)(k_2 + k_3B_1 + k_4B_2)}{(k_1 + k_3A_1 + k_4A_2)(h_2 + h_3B_1 + h_4B_2) - (k_2 + k_3B_1 + k_4B_2)(h_1 + h_3A_1 + h_4A_2)}\right]$$

$$Y_{12} = \frac{-Y_gY_d}{(h_1 + h_3A_1 + h_4A_2)} \times \left[1 + \frac{(h_2 + h_3B_1 + h_4B_2)(k_1 + k_3A_1 + k_4A_2)}{(k_2 + k_3B_1 + k_4B_2)(h_1 + h_3A_1 + h_4A_2) - (k_1 + k_3A_1 + k_4A_2)(h_2 + h_3B_1 + h_4B_2)}\right]$$

$$Y_{21} = \frac{-Y_d}{(h_2 + h_3B_1 + h_4B_2)} \left[-(h_3C_1 + h_4C_2) + (h_1 + h_3A_1 + h_4A_2) \times \frac{(k_3C_1 + k_4C_2)(h_2 + h_3B_1 + h_4B_2) - (h_3C_1 + h_4C_2)(k_2 + k_3B_1 + k_4B_2)}{(k_2 + k_3A_1 + k_4A_2)(h_2 + h_3B_1 + h_4B_2) - (k_2 + k_3B_1 + k_4B_2)(h_1 + h_3A_1 + h_4A_2)}\right]$$

$$Y_{22} = Y_d \left[1 + \frac{Y_d(k_1 + k_3A_1 + k_4A_2)}{(k_2 + k_3B_1 + k_4B_2)(h_1 + h_3A_1 + h_4A_2) - (k_1 + k_3A_1 + k_4A_2)(h_2 + h_3B_1 + h_4B_2)}\right]$$

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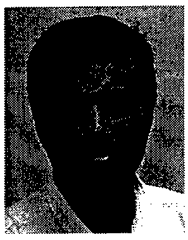

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